REMARKS

Applicants respectfully request reconsideration of the pending claims. In that regard, consider Applicants' Figure 2, which illustrates (in accordance with claim 1) an exemplary delay-matched ASIC conversion of the FPGA shown in Figure 1. The FPGA has nine logic blocks labeled as PFUs 00 through 22. As known in the art, these logic blocks may be LUT-based logic blocks. For example, each logic block may have 8 LUTs, each LUT having a flip-flop (FF) that may register the combinatorial output from the LUT. This same architecture is implemented in the ASIC conversion of Figure 2: there are nine logic blocks, each having 8 LUT-FF combinations. Because the ASIC logic blocks have the same architecture and placement as in the FPGA logic block, the delay matching problems of the prior art are avoided. Moreover, not only are the ASIC logic blocks matched to the FPGA logic blocks, the routing structure is also matched in that it is designed to provide the same couplings and propagation delays as the FPGA routing structure.

Powell stands in sharp contrast: As seen in Figure 9, Powell discloses a conventional mask programmable circuit, in which there are no logic blocks corresponding to the logic blocks of an FPGA., just an array of logic gates. Powell recognizes this distinction between logic blocks and logic gates by denoting the programmed gates that correspond to an FPGA logic block as a "soft-CLB."

> Typically, it is necessary to interconnect a number of logic gates on the MPGA substrate in order to realized equivalent logic function performed by a particular CLB in the FPGA implementation. In the MPGA implementation, this block of logic does not have hard or physically defined boundaries as does its corresponding CLB in the FPGA implementation, and thus it shall be referred to hereinafter and in the claims as a "Soft-CLB", to indicates its virtual character.
> (Col. 8, lines 15-24).

Because Powell has no logic blocks having the same architecture and placement as logic blocks in the FPGA-to-be-converted, Powell must then practice considerable

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machinations to attempt to match the delays within the FPGA logic blocks and the delays within the FPGA routing structure. Applicants' claimed ASIC conversion, on the other hand, has "hard" (rather than soft) logic blocks that physically correspond to the FPGA logic blocks on a one-to-one basis. Because of this physical correspondence, the routing structure will also correspond to the routing structure used in the FPGA. Delay matching is thus an intrinsic feature of Applicants' conversion. In contrast, because Powell's "soft CLBs" do not physically correspond to the FPGA logic blocks being converted, Powell's routing structure will necessarily have a different layout than the FPGA being converted.

Accordingly, claim 1 and its dependent claims 2 – 13 are allowable over the Powell reference. Similarly, independent claims 17, 32, 38 and 41 and their corresponding dependent claims are allowable for analogous reasons.

CONCLUSION

For the foregoing reasons, Applicants respectfully submit that Claims 1 – 13, 17 – 20, and 32 – 37 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Commissioner for Patents, Fax No. 571-273-8300 on the date stated below.

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Respectfully submitted,

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